Fermi National Accelerator Laboratory

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Engineering Note

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Project: D0 Tracking Electronics
Doc. No: U970919A

Subject: Test Beam DAQ Findings

Problem	Solution
1) Corruption of SVX initialization bits	Install 6" wide copper from Port Card crate to SVXs
2) Incorrect SVX initialization	Delay SVX clock to increase TNBR setup time
3) Late & narrow DVALID pulse for Chip ID	Delay SVX clock to increase TNBR setup time
4) Bad bits in readout cycle of SVXs	• Careful termination of DVALID • Install adjustable delays on DVALID • Minimize length of "Y" cable extensions • Added copper tape Gnd plane to small cable extension • Add clock driver local to SVX
5) SVX latchup during cycle	Add clock driver local to SVX
6) Clock noise on SVX input for VLPC	Remove clock driver local to SVX
7) Extra word between chips during readout	Delayed reading FIFO by ~12 clocks (Chips skip one clock when passing priority, but no clocks are skipped in reading the FIFO)
8) G-Link loss of lock Port	Combination of careful layout techniques in next Card.